PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-350202

(43)Date of publication of application : 15.12.2000

(51)Int.Cl. H04N 7/24
H03M 7/30
H04N 1/409
H04N 1/41
H04N 1/415

(21)Application number : 11-355563

(22)Date of filing : 15.12.1999

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(30)Priority

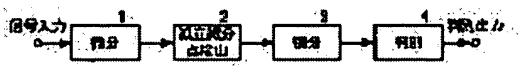
Priority number : 11083190 Priority date : 26.03.1999 Priority country : JP

(54) BLOCK NOISE DETECTING DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To accurately detect a block noise even when a decoder does not output a signal indicating the border of pixel blocks.

SOLUTION: A differentiating circuit 1 outputs a differentiated signal according to an input video signal and an isolated differentiation point detecting circuit 2 detects an isolated differentiation point of the differentiated signal. Then an integrating circuit 3 performs an integrating process. The integrating circuit 3 performs the integrating process in cycles of pixel blocks and cumulatively adds information on isolated differentiation points generated in pixel block cycles. A decision circuit 4 decides whether or not there is a block noise for each frame according to the output of the integrating circuit 3.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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04/8052-SNY

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報**（Ａ）　(11)特許出願公開番号
特開2000－350202
（P2000－350202A）
(43)公開日　平成12年12月15日(2000.12.15)

(51)Int.Cl.⁷		識別記号	FI			テーマコード（参考）
H04N	7/24		H04N	7/13	Z	5C059
H03M	7/30		H03M	7/30	A	5C077
H04N	1/409		H04N	1/41	Z	5C078
	1/41			1/415		5J064
	1/415			1/40	101C	9A001

審査請求　未請求　請求項の数３　ＯＬ　（全 6 頁）

(21)出願番号　特願平11－355563
(22)出願日　平成11年12月15日(1999.12.15)
(31)優先権主張番号　特願平11－83190
(32)優先日　平成11年３月26日(1999.3.26)
(33)優先権主張国　日本（ＪＰ）

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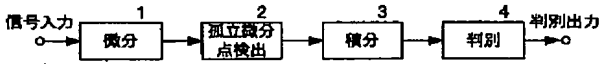
(54)【発明の名称】　ブロックノイズ検出装置

(57)【要約】
【課題】　デコーダが画素ブロックの境界を示す信号を出力しない場合であっても、ブロックノイズを正確に検出できるようにする。
【解決手段】　微分回路１は入力映像信号に基づき微分信号を出力し、孤立微分点検出回路２で微分信号における孤立微分点が検出される。その後、積分回路３で積分処理が施される。積分回路３では、画素ブロックの周期で積分処理が行われ、画素ブロック周期で発生している孤立微分点の情報が累積加算される。判別回路４は積分回路３の出力に基づきブロックノイズの有無をフレーム単位で判別する。



【特許請求の範囲】
【請求項1】所定の矩形ブロック単位で圧縮伸張処理された映像信号におけるブロックノイズを検出するためのブロックノイズ検出装置であり、
入力映像信号を微分処理して微分信号を得る微分手段と、
前記微分手段からの微分信号におけるインパルス状のパルスを検出してこれを孤立微分点検出信号として出力する孤立微分点検出手段と、
前記微分手段からの孤立微分点検出信号に積分処理を施す積分手段と、
前記積分手段の出力と所定のしきい値とを用いてブロックノイズ発生の有無を判別する判別手段とを有することを特徴とするブロックノイズ検出装置。
【請求項2】前記積分手段は、前記孤立微分点検出手段の出力する孤立微分点検出信号を前記所定の矩形ブロックの周期で積分処理し、
前記判別手段は、画面単位で前記積分手段の出力を計数することによりブロックノイズ発生の有無を判別することを特徴とする請求項１記載のブロックノイズ検出装置。
【請求項3】前記積分手段は、前記孤立微分点検出手段の出力する孤立微分点検出信号を水平方向及び垂直方向に積分処理することを特徴とする請求項２記載のブロックノイズ検出装置。
【発明の詳細な説明】
【0001】
【発明の属する技術分野】本発明は、映像信号を画素ブロック単位で符号化及び復号化した際に生じるブロックノイズを検出するためのブロックノイズ検出装置に関する。
【0002】
【従来の技術】映像信号を圧縮符号化する際に、水平及び垂直方向に隣接する複数の画素を１つの矩形ブロック（以下、画素ブロックと記す）として、この画素ブロック内での隣接画素の相関の高さを利用して画素ブロック単位で圧縮符号化を施す圧縮符号化方式が広く知られている。そして、このような圧縮符号化方式により圧縮符号化処理が施された圧縮映像信号は、記録媒体あるいは伝送路等を介した後に、圧縮符号化時とは相補的な伸張処理が画素ブロック単位で施され、元の映像信号が復元される。
【0003】また、このような圧縮符号化及び復号化方式では、記録媒体あるいは伝送路における映像信号の情報量を小さく抑えたい場合には、圧縮効率が高めに設定され、また映像信号を高画質のまま維持したい場合には、圧縮効率が低めに設定される。
【0004】ところが、圧縮効率を高めに設定して情報量を小さく抑えた場合、画素ブロック単位で隣接ブロックとの間に階調差が生じることがある。特に階調変化の緩やかな映像信号部分では、この隣接ブロック間での階調差が目に付き易くなる。なお、このような隣接ブロック間での階調差によるノイズは一般的にブロックノイズと呼ばれている。
【0005】また、記録媒体を介して再生させた映像信号では、例えば記録再生ヘッドの汚れ、摩耗等が原因でこのブロックノイズが発生することがあり、このような記録再生処理に伴うブロックノイズもまた画面上で目に付き易い。
【0006】このようにして画面上に発生したブロックノイズを目立たないようにする方法としては、これまで様々な方法が考えられてきたが、その一例として、ブロックノイズの発生している画素ブロックとその隣接ブロックとの境界部分を補間及びその他の処理にて平滑化する方法が知られている。
【0007】図６は、画素ブロックの境界部分に一列に配列された４つの画素ｘ１乃至ｘ４の信号レベルを示すものであり、画素ｘ１及びｘ２が同一画素ブロック内の画素、また画素ｘ３及びｘ４が同一画素ブロック内の画素であり、夫々の画素ブロックが隣接している状態を示している。
【0008】同図に示す如く、画素ｘ１とｘ２との信号レベルの差はｄ１、そして画素ｘ３とｘ４との信号レベルの差はｄ３であるのに対して、隣接画素である画素ｘ２とｘ３との信号レベルの差はｄ１、ｄ２に比して非常に大きいｄ２となっており、ブロックノイズが発生していることがわかる。このようなブロックノイズの発生を、これまでは画素ブロックの境界部分における信号レベルを比較することにより検出し、これを補正していた。
【0009】
【発明が解決しようとする課題】このように、映像信号における画素ブロックの境界が明らかな場合、その境界部分の画素の信号レベルを比較することにより、ブロックノイズの発生を検出することが可能であるが、画素ブロックの境界部分が明らかでない場合には、まず画素ブロックの境界部分を入力映像信号から検出しなければならず、この検出が正確でない場合には、当然の如くブロックノイズの適切な補正を行うことが不可能であった。
【0010】即ち、圧縮映像信号の伸張処理を行うデコーダが画素ブロックの境界を示すパルスを出力する場合には、このパルスに基づきブロックノイズの検出が可能であるが、このデコーダが境界を示すパルスを出力しない場合には、以上のようなブロックノイズの適切な検出及び補正を行うことが不可能であった。
【0011】
【課題を解決するための手段】本発明に係るブロックノイズ検出装置は、所定の矩形ブロック単位で圧縮伸張処理された映像信号におけるブロックノイズを検出するためのブロックノイズ検出装置であり、入力映像信号を微分処理して微分信号を得る微分手段と、前記微分手段か

らの微分信号におけるインパルス状のパルスを検出してこれを孤立微分点検出信号として出力する孤立微分点検出手段と、前記微分手段からの孤立微分点検出信号に積分処理を施す積分手段と、前記積分手段の出力と所定のしきい値とを用いてブロックノイズ発生の有無を判別する判別手段とを有することを特徴とするものである。

【0012】また、前記積分手段は、前記孤立微分点検出手段の出力する孤立微分点検出信号を前記所定の矩形ブロックの周期で積分処理し、前記判別手段は、画面単位で前記積分手段の出力を計数することによりブロックノイズ発生の有無を判別することを特徴とするものである。

【0013】また、前記積分手段は、前記孤立微分点検出手段の出力する孤立微分点検出信号を水平方向及び垂直方向に積分処理することを特徴とするものである。

【0014】

【発明の実施の形態】図１は本発明に係るブロックノイズ検出装置を説明するためのブロック図、図２は図１で示したブロックノイズ検出装置の微分処理及び孤立微分点検出処理の動作を示す図であり、本発明に係るブロックノイズ検出装置は、入力映像信号の画素ブロックの境界が明らかでない場合でも、ブロックノイズを正確に検出できることを特徴としている。

【0015】図１において、１は入力映像信号を微分処理する微分回路、２は微分回路１から出力される微分信号における孤立微分点を検出する孤立微分点検出回路である。

【0016】また、３は孤立微分点検出回路２にて得られた孤立微分点検出信号を積分処理する積分回路、４は積分回路３にて積分処理された積分信号に基づきブロックノイズの存在するフレームを判別する判別回路である。

【0017】以下、図１と図２とを用いて、本発明に係るブロックノイズ検出装置の孤立微分点検出までの動作を説明する。なお、図２は水平方向８画素×垂直方向８画素により１つの画素ブロックが構成される入力映像信号からブロックノイズを検出した例を示しており、同図では、５画素ブロック分の映像信号が示されている。

【0018】図２において（ａ）は微分回路１の入力信号を示しており、微分回路１は入力信号を微分処理した（ｂ）に示す如く微分信号を出力する。その後、孤立微分点検出回路２では、微分信号におけるインパルス状のパルスのみが検出されて（ｃ）に示す如く孤立微分点検出信号を出力する。

【0019】次に、積分回路３及び判別回路４の詳細について、図３を用いて説明する。孤立微分点検出回路２で検出された孤立微分点検出信号は、値変換回路３ａに入力され、値変換回路３ａは孤立微分点検出信号がＨのタイミングで１の値を出力し、Ｌのタイミングで（－１）の値を出力する。

【0020】そして、値変換回路３ａの出力は加算器３ｂに入力され、第１のリミッタ３ｄは、加算器３ｂの出力を上限値及び下限値を設けつつ出力し、第１のリミッタ３ｄの出力が遅延素子３ｃで８画素分遅延された後に、加算器３ｂで値変換回路３ａの出力と加算処理される。

【0021】つまり、ここで示すブロックノイズ検出回路では、水平方向８画素及び垂直方向８画素の全６４画素により画素ブロックが構成されている場合の映像信号を想定して、遅延素子３ｃでの遅延量を８画素分に設定してある。

【0022】そして、第１のリミッタ３ｄは、加算器３ｂの出力を上限値及び下限値を設けつつ出力し、第１のコンパレータ３ｅは第１のリミッタ３ｄの出力をその内部に保持している規定値と比較し、第１のリミッタ３ｄの出力が規定値より大きい場合は１の値、規定値以下の場合は（－１）の値を出力する。このような第１のコンパレータ３ｅまでの処理により、孤立微分点検出信号が水平方向に８画素周期で累積加算され、孤立微分点検出信号の水平方向の積分値が出力される。

【0023】次に、第１のコンパレータ３ｅの出力は加算器３ｆに入力され、第２のリミッタ３ｈは加算器３ｆの出力を上限値及び下限値を設けつつ出力し、第２のリミッタ３ｈの出力が遅延素子３ｇで１水平ライン期間分遅延させれ後に、加算器３ｆで第１のコンパレータ３ｅの出力と加算処理される。

【0024】そして、第２のリミッタ３ｈは、加算器３ｆの出力を上限値及び下限値を設けつつ出力し、第２のコンパレータ３ｉは第２のリミッタ３ｈの出力をその内部に保持している規定値と比較し、第２のリミッタ３ｈの出力が規定値より大きい場合は１の値、規定値以下の場合は（－１）の値を出力する。このような第２のコンパレータ３ｉまでの処理により、孤立微分点検出信号が水平方向に８画素周期且つ垂直方向に累積加算され、孤立微分点検出信号の水平方向及び垂直方向の積分値が出力される。

【0025】そして、判別回路４におけるカウンタ４ａは第２のコンパレータ３ｉの出力する１の値をカウントし、１画面毎にそのカウント数を出力することにより、１画面内に発生しているブロックノイズの度合いに応じた信号を出力する。そして、第３のコンパレータ４ｂでは、カウンタ４ａの出力値をその内部に保持している規定値と比較して、カウンタ４ａの出力が規定値より大きい場合はブロックノイズの存在するフレームであることを示す１の値、規定値以下の場合はブロックノイズの存在しないフレームであることを示す（－１）の値を出力する。

【0026】次に図３及び図４を用いて積分回路３及び判別回路４の動作を更に詳しく説明する。図４において、１－１乃至４－６は、夫々水平方向８画素×垂直方向８画素により構成される画素ブロックを示しており、画素ブロック１－３乃至１－６、画素ブロック３－１乃至３－４ではブロックノイズが発生しているものとする。

【0027】また、図４において、○印は第１のコンパレータ３ｅが１の値を出力する一方第２のコンパレータ３ｉが（－１）の値を出力する画面位置、△印は第１のコンパレータ３ｅが（－１）の値を出力する一方第２のコンパレータ３ｉが１の値を出力する画面位置、□印は第１のコンパレータ３ｅ、第２のコンパレータ３ｉ共に１の値を出力する画面位置を示している。

【0028】値変換回路３ａには、まず画素ブロック１－１乃至１－６の先頭ラインにおける孤立微分点検出信号が入力され、加算器３ｂ、第１のリミッタ３ｄ、遅延素子３ｃで形成される加算ループにより孤立微分点検出信号が水平方向に８画素周期で累積加算され、先頭ラインの処理を終えると次のラインにおける処理が開始される。

【0029】ここで、画素ブロック１－１及び１－２ではブロックノイズが発生していない。このような、画素ブロックの部分では水平方向に隣接する画素に信号レベル差が生じ、孤立微分点検出信号でＨが出力されることはあるが、このＨの出力が８画素周期で継続的に発生することはないため、第１のリミッタ３ｄの出力は、画素ブロック１－２と１－３との境界、１－３と１－４との境界、１－４と１－５との境界、１－５と１－６との境界でのみその出力値が上昇する傾向にある。

【0030】そして、ここでは、２ライン目における画素ブロック１－３と１－４との境界での処理を行った際に第１のリミッタ３ｄの出力値が第１のコンパレータ３ｅ内に保持されている値を超えて、第１のコンパレータ３ｅが１の値を出力し、第９ライン目における画素ブロック２－４と２－５との境界部分までは各ブロックの境界部分で１の値を出力する。

【0031】なお、画素ブロック２－１乃至２－６ではブロックノイズが発生していないため、９ライン目以降の画素ブロックの境界部分では、第１のリミッタ３ｄの出力値が減少する傾向にあるが、９ライン目の画素ブロック２－５と２－６との境界部分で第１のリミッタ３ｄの出力値が第１のコンパレータ３ｅ内に保持されている値以下となり、それ以降第１のコンパレータ３ｅは各ブロックの境界部分で（－１）の値を出力する。

【0032】また、同様に画素ブロック３－１乃至３－４でもブロックノイズが発生しているため、１７ライン目以降、各画素ブロックの境界にて第１のリミッタ３ｄの出力値が上昇する傾向にあり、１８ライン目の画素ブロック３－２と３－３との境界部分から２５ライン目の画素ブロック４－３と４－４の境界部分までは各ブロックの境界部分で第１のリミッタ３ｄの出力値が第１のコンパレータ３ｅ内に保持されている値を超えて、第１のコンパレータ３ｅが１の値を出力する。

【0033】一方、加算器３ｆ、第２のリミッタ３ｈ、遅延素子３ｇで形成される加算ループでは第１のコンパレータ３ｅの出力する値が垂直方向に累積加算されるため、ブロックノイズが発生している画素ブロックの境界部分では、第２のリミッタ３ｈの出力値が上昇し、第２のリミッタ３ｈの出力が第２のコンパレータ３ｉの内部に保持される値を超えると、第２のコンパレータ３ｉが１の値を出力する。

【0034】つまり、図４の例では、２ライン目の画素ブロック１－３と１－４との境界部分以降、第１のコンパレータ３ｅは、各ブロックの境界部分において１の値を出力し続けているため、第２のリミッタ３ｈの出力値は上昇し、５ライン目の画素ブロック１－３と１－４との境界部分で第２のリミッタ３ｈの出力値が第２のコンパレータ３ｉの内部に保持される値を超えて、第２のコンパレータ３ｉが１の値を出力する。

【0035】そして、９ライン目の画素ブロック２－５と２－６との境界部分以降、第１のコンパレータ３ｅは画素ブロックの境界部分において（－１）の値を出力しているため、第２のリミッタ３ｈの出力値が減少し、１２ライン目の画素ブロック２－５と２－６との境界部分で第２のリミッタ３ｈの出力値が第２のコンパレータ３ｉの内部に保持される値以下となり、それ以降第２のコンパレータ３ｉは各ブロックの境界部分で（－１）の値を出力する。

【0036】また、同様に画素ブロック３－１乃至３－４でもブロックノイズが発生しているため、１８ライン目の画素ブロック３－２と３－３との境界部分以降、各画素ブロックの境界にて第２のリミッタ３ｈの出力値が上昇傾向にあり、２１ライン目の画素ブロック３－２と３－３との境界部分から２８ライン目の画素ブロック４－３と４－４の境界部分までは各ブロックの境界部分で第２のリミッタ３ｈの出力値が第２のコンパレータ３ｉ内に保持されている値を超えて、第２のコンパレータ３ｉが１の値を出力する。

【0037】そして、カウンタ４ａは、第２のコンパレータ３ｉが１の値を出力した回数を１画面内でカウントする。同図に示す例では、カウンタ４ａのカウント値は７４となり、このカウンタ４ａの出力するカウント値と第３のコンパレータ４ｂの内部に保持される値を超えているか否かで、画面内のブロックノイズの有無が判別され、その判別結果が出力される。

【0038】また、この判別結果に基づき、ブロックノイズの存在する画面のみブロックノイズの低減処理を行う場合、判別結果がフレーム単位で細かく切り替わるとかえって見辛い映像となってしまうことがある。従って、図５に示す如く判別回路４内に遅延素子４ｃ及び４ｄ、そしてメジアン回路４ｅを設けることによりこのようなチャタイリングを防止することができる。

【0039】つまり、カウンタ４ａの出力を遅延素子４ｃで１画面（フレーム）分遅延して出力し、更に、遅延素子４ｄで１画面（フレーム）分遅延して出力することにより、連続する３画面（フレーム）分のカウント値をメジアン回路４ｅに入力し、メジアン回路４ｅでは、入力さ

れる３値のうちの中間値を第３のコンパレータ４ｂに出力するため、例えば映像信号がフレーム間圧縮を行うＭＰＥＧ圧縮信号のような場合でも、若干のシステリシス特性をもたせることにより、良好なブロックノイズの低減処理を行うことができる。

【0040】このように、本発明に係るブロックノイズ検出装置は、ブロックノイズが発生した際に、このブロックノイズの周辺における画素の信号レベルに急峻なレベル差が発生し微分波形が特徴的になることと、このレベルの変動が画素ブロックの単位で周期性をもって発生することに着目してブロックノイズを検出している。

【0041】なお、積分回路３における積分特性は、画素ブロックの大きさに応じて適宜設定可能であり、この積分特性を調整することによりブロックノイズの検出の精度が高められることは言うまでもない。

【0042】また、以上の実施例では、積分回路３にて孤立微分点検出信号を水平方向及び垂直方向に積分処理した例を示したが、水平方向にのみ積分処理しても構わない。その場合には、第１のコンパレータ３ｅの出力をそのままカウンタ４ａに入力し、第１のコンパレータ３ｅの出力する１の値の数により画面内のブロックノイズの有無を判別すれば良い。

【0043】また、以上の実施例では、本発明に係るブロックノイズ検出装置がハードウェアにより構成されるものとして説明したが、同様の処理をソフトウェア処理により行っても構わない。また、本ブロックノイズ検出装置の構成をパソコンで代用することも可能である。つまり、パソコン内のハードディスク上のアプリケーション記録領域にＣＤ－ＲＯＭあるいはネットワークを介して提供される上記処理プログラムをインストールし、このアプリケーションプログラムとＣＰＵとの間で図１に示す構成の処理を行うことで、パソコンにより本発明に係るブロックノイズ検出装置を構成できる。

【0044】

【発明の効果】本発明に係るブロックノイズ検出装置によれば、入力映像信号に微分処理を施し、この微分信号におけるインパルス状のパルスを検出した孤立微分点検出信号を積分処理することによりブロックノイズが検出されるため、画素ブロックの境界が明らかでない場合であってもブロックノイズの有無を正確に判別できるという効果を奏する。また、この積分処理を水平方向及び垂直方向に行うため、ブロックノイズにより発生した水平方向及び垂直方向に相関のあるインパルス状のパルスを適切に検出でき、ブロックノイズの有無を正確に判別できるという効果を奏する。

【図面の簡単な説明】

【図１】本発明に係るブロックノイズ検出装置を説明するためのブロック図である。

【図２】微分処理及び孤立微分点検出処理を説明するための図である。

【図３】積分回路及び判別回路の詳細を示す図である。

【図４】積分回路及び判別回路の動作を説明するための図である。

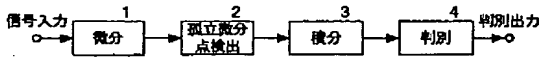
【図５】判別回路の他の例を示す図である。

【図６】画素ブロックの境界部分における信号レベルの差を示す図である。

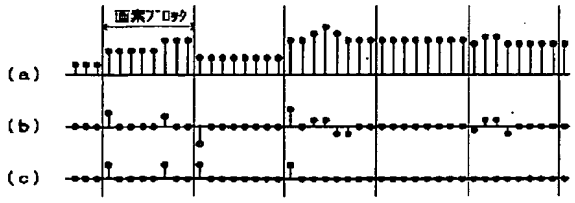
【符号の説明】

１…微分回路
２…孤立微分点検出回路
３…積分回路
３ａ…値変換回路
３ｂ、３ｆ…加算器
３ｃ、３ｇ…遅延素子
３ｄ…第１のリミッタ
３ｅ…第１のコンパレータ
３ｈ…第２のリミッタ
３ｉ…第２のコンパレータ
４…判別回路
４ａ…カウンタ
４ｂ…第３のコンパレータ
４ｃ、４ｄ…遅延素子
４ｅ…メジアン回路

【図１】



【図２】



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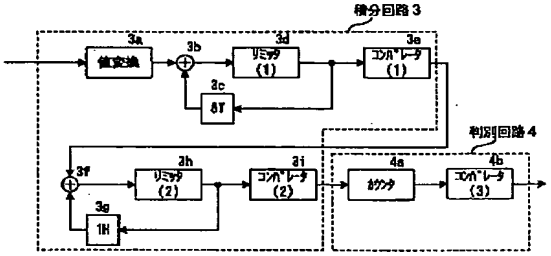
【図３】



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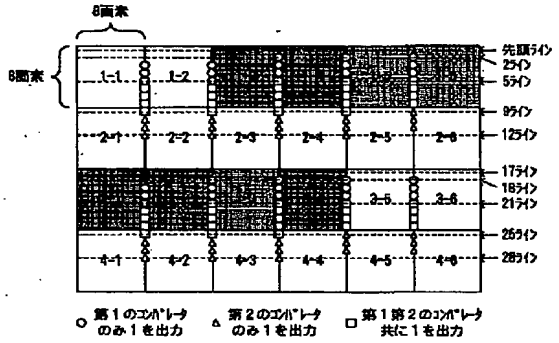

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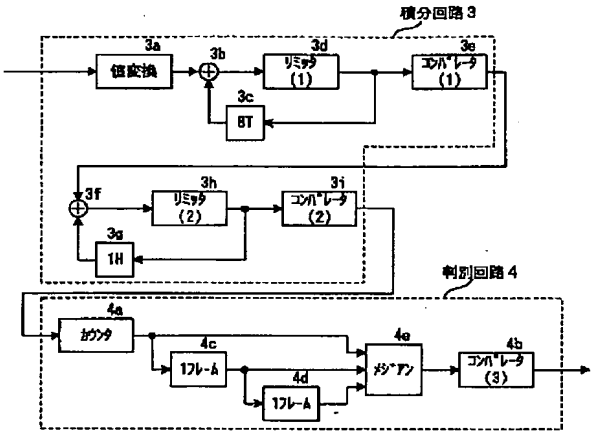
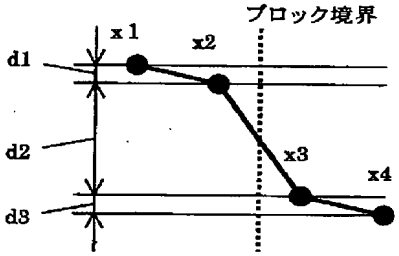


【図６】



フロントページの続き

Ｆターム(参考) 5C059 KK03 LC03 MA21 SS06 SS11
UA02 UA21
5C077 LL02 NN02 PP47 PP48 PQ17
PQ20 PQ24 PQ25
5C078 AA04 BA44 CA21 DA22
5J064 AA01 BA15 BB00 BC02 BC08
BC10 BC14 BC24 BD01
9A001 EE04 HH23

04/8052-SNY

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 039 760 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
27.09.2000 Bulletin 2000/39

(51) Int. Cl.[7]: **H04N 7/30**

(21) Application number: **00302014.6**

(22) Date of filing: **13.03.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **26.03.1999 JP 8319099**
20.10.1999 JP 29791599
15.12.1999 JP 35556399

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(54) Apparatus and method of block noise detection and reduction

(57) Block noises generated on an input video signal that has been code and decoded per pixel block are detected. The input video signal is differentiated per pixel block to obtain a differentiated signal. Impulses of the differentiated signal is detected to obtain a detection signal carrying the impulses. The detection signal is integrated and compared with a reference signal to determine whether the block noise is generated on the input video signal. For noise reduction, the detection signal is filtered to obtain a correction signal. The input video signal is delayed by a predetermined period. The correction signal is added to the delayed video signal to cancel the difference in signal level on the boundary between a first pixel block on which a block noise is generated and a second pixel block adjacent to the first pixel block of the input video signal.

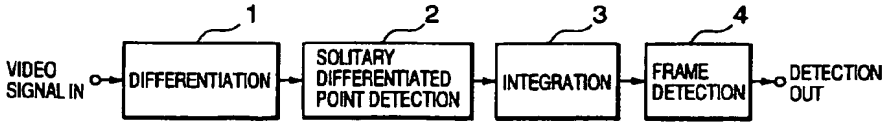

FIG.2

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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to detection and reduction of block noises generated when video signals are coded and decoded per pixel block.

[0002] A well known encoding technique is to compress video signals per pixel block with exploiting correlation between adjacent pixels within each block. Each pixel block consists of a predetermined number of pixels in the horizontal and the vertical directions.

[0003] The coded video signals are stored in a storage medium or transferred to a decoding apparatus via a transfer cable. After storage or transfer, the coded video signals are expanded per pixel block for decoding.

[0004] The lower the compression ratio, the higher the image quality. On the other hand, the higher the compression ratio, the smaller the amount of video data stored in a storage medium or transferred along a transfer cable. High compression ratio would however cause a difference in gradation between adjacent pixel blocks. The gradation difference is called a block noise and noticeable on video signal portions with small gradation changes.

[0005] Block noises would also be generated when video signals are reproduced from a storage medium by a dirty or worn-out magnetic head. These noises are also noticeable on a monitor.

[0006] Several techniques have been developed for detection and reduction of block noises.

[0007] One of the techniques is to smooth the boundary between adjacent pixel blocks over which block noises are generated, by interpolation, as shown in FIG. 1.

[0008] This figure shows signal levels of four pixels x1 to x4 aligned over the boundary between pixel blocks BK1 and BK2.

[0009] The difference in signal level between the pixels x1 and x2 in the block BK1 is d1, and that between x3 and x4 in the block BK2 is d3. The signal difference between the pixels x2 and x3 adjacent to each other over the block boundary is d2. The difference d2 is larger than d1 and d3, thus causing generation of block noises.

[0010] The block noise can be detected by comparison of signal level over the block boundary for reduction if the boundary is already known. If not, however, the block boundary must to be detected from an input video signal.

[0011] Such noise reduction requires precise boundary detection by, for example, a decoding apparatus capable of outputting pulse signals that indicate pixel block boundaries.

[0012] Japanese Unexamined Patent Publication Nos. 1991(3)-174891 and 1996(8)-149470 disclose other techniques for detecting and reducing block noises. These techniques however require a bulk of circuitry.

SUMMARY OF THE INVENTION

[0013] A purpose of the present invention is to provide an apparatus and a method of detection and reduction of block noises with no requirement of detecting pixel block boundaries of an input video signal.

[0014] Another purpose of the present invention is to provide an apparatus for detecting and reducing block noises with relatively small circuitry.

[0015] The present invention provides an apparatus for detecting a block noise generated on an input video signal that has been code and decoded per pixel block. The apparatus includes: a differentiator to differentiate the input video signal per pixel block to obtain a differentiated signal; a detector to detect impulses of the differentiated signal to obtain a detection signal carrying the impulses; an integrator to integrate the detection signal; and a determinator to compare the detection signal and a reference signal to determine whether the block noise is generated on the input video signal.

[0016] Furthermore, the present invention provides an apparatus for reducing a block noise generated on an input video signal that has been code and decoded per pixel block. The apparatus includes: a differentiator to differentiate the input video signal per pixel block to obtain a differentiated signal and detect impulses of the differentiated signal, thus outputting a detection signal carrying the impulses; a filter to filter the detection signal to obtain a correction signal; a delay section to delay the input video signal by a predetermined period; and an adder to add the correction signal to the delayed video signal to cancel a difference in signal level on the boundary between a first pixel block on which a block noise is generated and a second pixel block adjacent to the first pixel block of the input video signal.

[0017] Moreover, the present invention provides a method of detecting a block noise generated on an input video signal that has been code and decoded per pixel block. The input video signal is differentiated per pixel block to obtain a differentiated signal. Impulses of the differentiated signal are detected to obtain a detection signal carrying the impulses. The detection signal is integrated. The integrated detection signal is compared with a reference signal to determine whether the block noise is generated on the input video signal.

[0018] The present invention further provides a method of reducing a block noise generated on an input video signal that has been code and decoded per pixel block. The input video signal is differentiated per pixel block to obtain a differentiated signal and detect impulses of the differentiated signal, thus outputting a detection signal carrying the impulses. The detection signal is filtered to obtain a correction signal. The input video signal is delayed by a predetermined period. The correction signal is added to the delayed video signal to cancel a difference in signal level on the boundary

between a first pixel block on which a block noise is generated and a second pixel block adjacent to the first pixel block of the input video signal.

[0019] The present invention still provides a computer-implemented method of detecting a block noise generated on an input video signal that has been code and decoded per pixel block. The input video signal is differentiated per pixel block to obtain a differentiated signal. Impulses of the differentiated signal are detected to obtain a detection signal carrying the impulses. The detection signal is integrated. The integrated detection signal is compared with a reference signal to determine whether the block noise is generated on the input video signal.

[0020] The present invention also provides a computer-implemented method of reducing a block noise generated on an input video signal that has been code and decoded per pixel block. The input video signal is differentiated per pixel block to obtain a differentiated signal and detect impulses of the differentiated signal, thus outputting a detection signal carrying the impulses. The detection signal is filtered to obtain a correction signal. The input video signal is delayed by a predetermined period. The correction signal is added to the delayed video signal to cancel a difference in signal level on the boundary between a first pixel block on which a block noise is generated and a second pixel block adjacent to the first pixel block of the input video signal.

[0021] Furthermore, the present invention provides a processor readable medium storing program code for causing a computer to detect a block noise generated on an input video signal that has been code and decoded per pixel block. The processor readable medium stores: first program code means for differentiating the input video signal per pixel block to obtain a differentiated signal; second program code means for detecting impulses of the differentiated signal to obtain a detection signal carrying the impulses; third program code means for integrating the detection signal; and fourth program code means for comparing the integrated detection signal and a reference signal to determine whether the block noise is generated on the input video signal.

[0022] Moreover, the present invention provides a processor readable medium storing program code for causing a computer to reduce a block noise generated on an input video signal that has been code and decoded per pixel block. The processor readable medium stores: first program code means for differentiating the input video signal per pixel block to obtain a differentiated signal and detect impulses of the differentiated signal, thus outputting a detection signal carrying the impulses; second program code means for filtering the detection signal to obtain a correction signal; third program code means for delaying the input video signal by a predetermined period; and fourth program code means for adding the correction signal to the delayed video signal to cancel a difference in signal level on the boundary between a first pixel block on which a block noise is generated and a second pixel block adjacent to the first pixel block of the input video signal.

BRIEF DESCRIPTION OF DRAWINGS

[0023]

FIG. 1 illustrates a conventional technique for detecting and reducing block noises;

FIG. 2 shows a block diagram of a preferred embodiment of a block noise detection apparatus according to the present invention;

FIGS. 3A to 3C illustrate the differentiation and solitary differentiated points detection functions of the block noise detection apparatus shown in FIG. 2;

FIG. 4 shows block diagrams of the integrator circuit and the frame detector of the block noise detection apparatus shown in FIG. 2;

FIG. 5 illustrates the functions of the integrator circuit and the frame detector of the block noise detection apparatus shown in FIG. 2;

FIG. 6 shows a block diagram of a modification of the frame detector of the block noise detection apparatus shown in FIG. 2;

FIG. 7 shows a block diagram of a preferred embodiment of a block noise reduction apparatus according to the present invention;

FIG. 8 illustrates the solitary differentiated point detection according to the present invention;

FIG. 9 shows a block diagram of a filter for filtering a solitary differentiated point detection signal shown in FIG. 8;

FIGS. 10A to 10E illustrate the function of the block noise signal reduction apparatus shown in FIG. 7; and

FIG. 11 shows a block diagram of another preferred embodiment of a block noise reduction apparatus according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0024] Preferred embodiments according to the present invention will be disclosed with reference to the attached drawings.

[0025] FIG. 2 shows a block diagram of a preferred embodiment of a block noise detection apparatus according to the present invention.

[0026] An input video signal that has been coded and decoded per pixel block is differentiated by a differentiating circuit 1. The differentiated video signal is supplied to a solitary differentiated point detector 2.

[0027] The detector 2 outputs a detection signal that indicates solitary differentiated points on the differentiated video signal. The detection signal is integrated by an integrator circuit 3.

[0028] The integrated detection signal is supplied to a frame detector 4 for detection of a video frame carrying block noises.

[0029] The functions of the differentiating circuit 1 and the solitary differentiated point detector 2 are explained with reference to FIGS. 3A to 3C.

[0030] Illustrated in FIG. 3A are input video signal components for five pixel blocks to be supplied to the differentiating circuit 1. Each pixel block consists of eight pixels in both the horizontal and the vertical directions.

[0031] The differentiated video signal shown in FIG. 3B is output by the differentiating circuit 1 and supplied to the solitary differentiated point detector 2.

[0032] The detector 2 outputs the detection signal that carries impulses as shown in FIG. 3C and indicates solitary differentiated points on the differentiated video signal. The detection signal is supplied to the integrator circuit 3 and then the frame detector 4.

[0033] The integrator circuit 3 and the frame detector 4 are disclosed in detail with reference to FIG. 4.

[0034] The solitary differentiated points detection signal output by the detector 2 is supplied to a value converter 3a. The converter 3a outputs "1" when the detection signal is HIGH (FIG. 3C) while it outputs "-1" when the detection signal is LOW.

[0035] The output of the value converter 3a is supplied to an adder 3b whose output is then supplied to a limiter 3d having predetermined upper and lower limit levels.

[0036] The output of the limiter 3d is clipped at the upper and lower limit levels and supplied to a delay circuit 3c and delayed by eight pixels (8T). The delayed signal is supplied to the adder 3b and added to the output of the value converter 3a.

[0037] In FIG. 4, the delay circuit 3c delays the output of the limiter 3d by eight pixels for an input video signal that carries pixel blocks each consisting of 64 pixels (8 x 8 in the horizontal and the vertical directions).

[0038] The output of the limiter 3d is supplied to a comparator 3e and compared with a predetermined reference level. The comparator 3e outputs "1" when the output of the limiter 3d is higher than the reference level, while it outputs "-1" when the output is equal to or lower than the reference level.

[0039] By the signal processing of the integrator circuit 3 described so far, the solitary differentiated points detection signal is accumulated per eight pixels in the horizontal direction to gain an integrated value of the detection signal in the horizontal direction.

[0040] The output (integrated value in the horizontal direction) of the comparator 3e is supplied to an adder 3f and then to a limiter 3h having predetermined upper and lower limit levels.

[0041] The output of the limiter 3h is clipped at the upper and lower limit levels and supplied to a delay circuit 3g and delayed by one horizontal line period (1H). The delayed signal is supplied to the adder 3f and added to the output of the comparator 3e.

[0042] The output of the limiter 3h is supplied to a comparator 3i and compared with a predetermined reference level. The comparator 3i outputs "1" when the output of the limiter 3h is higher than the reference level, while it outputs "-1" when the output is equal to or lower than the reference level.

[0043] By the signal processing of the integrator circuit 3 described so far, in addition to the processing in the horizontal direction, the solitary differentiated points detection signal is accumulated per eight pixels also in the vertical direction to gain an integrated value of the detection signal in the horizontal and the vertical directions.

[0044] Next, the signal processing of the frame detector 4 is disclosed.

[0045] The output (integrated value in the horizontal and the vertical directions) of the comparator 3i is supplied to a counter 4a. The counter 4a counts the number of "1" output by the comparator 3i and outputs the counted number per video frame. The number counted by the comparator 4a per frame depends on the degree of generation of block noises for each frame.

[0046] The output (counted number) of the counter 4a is supplied to a comparator 4b and compared with a predetermined reference level. The comparator 4b outputs "1" when the output of the counter 4a is higher than the reference level, while it outputs "-1" when the output is equal to or lower than the reference level.

[0047] The output "1" of the comparator 4b indicates that block noises are generated on a frame, while the output "-1" indicates no generation of block noises.

[0048] The functions of the integrator circuit 3 and the frame detector 4 are illustrated in FIG. 5.

[0049] In FIG. 5, the numerals 1-1 to 4-6 represent pixel blocks each consisting of eight pixels in both the horizontal and the vertical directions.

[0050] It is assumed that block noises are generated on the pixel blocks 1-3, 1-4, 1-5 and 1-6, and also 3-1, 3-2, 3-3 and 3-4.

[0051] Furthermore, it is assumed that the signs ○, △ and □ in FIG. 5 indicate locations of a video frame according to the outputs of the comparators 3e and 3i (FIG. 4) as follows:

[0052] The signs ○ indicate portions of the frame where the outputs of the comparators 3e and 3i are "1" and "-1", respectively.

[0053] The signs △ indicate portions of the frame where the outputs of the comparators 3e and 3i are "-1" and "1", respectively.

[0054] The signs □ indicate portions at the frame where the outputs of the comparators 3e and 3i are both "1".

[0055] Firstly, the solitary differentiated points detection signal for the first line on the blocks 1-1 to 1-6 is supplied to the value converter 3a (FIG. 4).

[0056] The solitary differentiated points detection signal is accumulated per eight pixels in the horizontal

direction by the addition loop circuitry consisting of the adder 3b, limiter 3d and delay circuit 3c (FIG. 4).

[0057] This process goes to the next lines one by one.

[0058] No block noises are generated on the blocks 1-1 and 1-2 according to the assumption. In these blocks, pixels adjacent to each other in the horizontal direction have a difference in signal level. And hence a solitary differentiated points detection signal for the blocks 1-1 and 1-2 may be "H". It is however very rare that the level "H" is continuously output per eight pixels. The output of the limiter 3d therefore has a tendency to rise only on the borders between the blocks 1-2 and 1-3, 1-3 and 1-4, 1-4 and 1-5, and also 1-5 and 1-6.

[0059] The level "H" will be continuously output per eight pixels as the solitary differentiated points detection signal when block noises are generated on the blocks 1-1 and 1-2.

[0060] According to the assumption on the signs ○ and □, the limiter 3d goes beyond the reference level of the comparator 3e, so that the comparator 3e outputs "1" on the border between the blocks 1-3 and 1-4 on the second line. The comparator 3e continuously outputs "1" on the border between the blocks 2-4 and 2-5 from the second line to the ninth line, as shown in FIG. 5.

[0061] Since it is assumed that no block noises are generated on the blocks 2-1 to 2-6, the output of the limiter 3d has a tendency to lower on the block borders from the ninth line. The output of the limiter 3d becomes lower than the reference level of the comparator 3e on the border between the blocks 2-5 and 2-6 on the ninth line, so that the comparator 3e continuously outputs "-1" from that portion.

[0062] On the other hand, since it is assumed that block noises are generated on the blocks 3-1 to 3-4, the output of the limiter 3d has a tendency to rise on the block borders from the 18-th line. The output of the limiter 3d goes beyond the reference level of the comparator 3e from the border between the blocks 3-2 and 3-3 on the 18-th line to the border between the blocks 4-3 and 4-4 on the 25-th line. The comparator 3e thus continuously outputs "1" from the 18-th to 25-th line.

[0063] In FIG. 4, the addition loop circuitry consisting of the adder 3f, limiter 3h and delay circuit 3g accumulates the output of the comparator 3e in the vertical direction. The output of the limiter 3h rises on the block borders where block noises are generated. The comparator 3i then outputs "1" when the output of the limiter 3h goes beyond the reference level of the comparator 3i.

[0064] As described above, according to the assumption in this embodiment, the comparator 3e continuously outputs "1" from the second line on the border between blocks 1-3 and 1-4 to the ninth line on the border between blocks 2-4 and 2-5. The output of the limiter 3h thus rises and goes beyond the reference level of the comparator 3i on the border between blocks 1-3 and 1-4 on the fifth line, so that the comparator 3i outputs "1" on each block border.

[0065] On the other hand, the comparator 3e continuously outputs "-1" from the ninth line on the border between blocks 2-5 and 2-6. The output of the limiter 3h becomes lower than the reference level of the comparator 3i on the border between blocks 2-5 and 2-6 on the 12-th line, so that the comparator 3i outputs "-1" on each block border.

[0066] Since assumption is made such that block noises are generated on the blocks 3-1 to 3-4, the output of the limiter 3h has a tendency to rise from the 18-th line on the border between the blocks 3-2 and 3-3, and goes beyond the reference level of the comparator 3i from the 21-th line on the border between the blocks 3-2 and 3-3 to the 28-th line on the border between the blocks 4-3 and 4-4. The comparator 3i thus outputs "1".

[0067] The counter 4a counts the number of "1" output by the comparator 3i per frame. The counted value is 74 that corresponds to the total number of △ and □ in this example of FIG. 5.

[0068] The counted value of the counter 4a is compared with the reference level of the comparator 4b to determine whether block noises are generated on a video frame. As already described, the output "1" of the comparator 4b indicates that block noises are generated on a frame, while the output "-1" indicates no generation of block noises.

[0069] Next, a modification of the frame detector 4 of the block noise detection apparatus is disclosed with reference to FIG.6. This modification is suitable for a video signal according to the MPEG (Moving Picture Coding Experts Group) standard.

[0070] Elements shown in FIG. 6 that are the same as or analogous to elements shown in FIG. 4 are referenced by the same reference numbers and will not be explained in detail.

[0071] The output of the comparator 3i (FIG. 4) is supplied to the counter 4a (FIG. 6) and its output is supplied to a median circuit 4e.

[0072] Also supplied to the median circuit 4e are the output of a delay circuit 4c by which the output of the counter 4a (FIG. 6) has been delayed by one frame and also the output of a delay circuit 4d by which the output of the delay circuit 4c has been delayed by one frame.

[0073] In another word, the counted values for three continuous frames are supplied to the median circuit 4e.

[0074] The median circuit 4e outputs the middle value among the three counted values. The middle value is then supplied to the comparator 4b for detection of block noises.

[0075] In this modification, the median circuit 4e offers protection of reproduced images from chattering which would occur when the output of the comparator 4b changes frequently between "1" and "-1".

[0076] Such frequent change in level occurs, for example, when block noises are generated on B frames but not on an I frame of a group of sequential B, B, I, B, B frames of a video signal according to the MPEG standard where B and I denote a predictive-coded

frame and an intra-coded frame, respectively.

[0077] For such an MPEG video signal, the frame delay conducted by the delay circuits 4c and 4d (FIG. 6) applies the hysteresis characteristics to the output of the counter 4a and its middle value is output by the median circuit 4e. Reproduced images thus can be protected from chattering.

[0078] As described above, the present invention achieves block noise detection based on the facts that the differentiated signal output by the differentiating circuit 1 (FIG.2) is noticeable as shown in FIG. 3B due to abrupt change in signal level of pixels around which block noises are generated, and also the level change occurs cyclically per pixel block.

[0079] The integration characteristics of the integrator circuit 3 (FIG. 4) can be adjusted according to the size of pixel blocks for accurate block noise detection.

[0080] Furthermore, the solitary differentiated points detection signal is integrated in both the horizontal and the vertical directions by the integrator circuit 3 in FIG. 4. The integration process may however be proceeded in only the horizontal direction. In this case, the output of the comparator 3e is directly supplied to the counter 4a for block noise detection based on the value of "1" output by the comparator 3e and counted by the counter 4a.

[0081] Described next with respect to FIG. 7 is a preferred embodiment of a block noise reduction apparatus according to the present invention.

[0082] An input video signal (1) that has been coded and decode per pixel block is supplied to a solitary differentiated point detector 10. The detector 10 differentiates the input signal (1) and outputs a detection signal (2) that indicates a solitary differentiated point. The detection signal (2) is filtered by a filter 20 and supplied to an adder 40.

[0083] The input video signal (1) is also supplied to a delay unit 30. The input signal (1) is delayed by a predetermined period and supplied to the adder 40. The adder 40 adds the output signals (3) and (4) of the filter 20 and the delay unit 30, respectively, to output a signal (5).

[0084] Illustrated in FIG. 8 is an example of the solitary differentiated point detection.

[0085] The solitary differentiated point detector 10 has a logical filter that filters the input video signal (1) to output an impulse signal as shown in FIG. 8 as the detection signal (2).

[0086] The detector 10 differentiates the input video signal (1) and compares the differentiated values (a, b, c, d and e) of adjacent pixels to output the differentiated value (c) of the pixel, which juts out compared to the values of other pixels.

[0087] In detail, in this example, the detector 10 outputs the value (c) that satisfies the condition $|c - d| > |d - e|$ and $|b - c| > |a - b|$ but does not satisfy the condition $b \leqq c \leqq d$ and $b \geqq c \geqq d$. The detection of the solitary differentiated point can also be conducted by the same way as illustrated in FIGS. 3A to 3C.

[0088] The value (c) is then supplied as the detection signal (2) to the filter 20 (FIG. 7) a block diagram of which is shown in FIG. 9.

[0089] The detection signal (2) is delayed by delay elements 2a to 2d by a period (T) that corresponds to one pixel for each delay element, totally five pixels.

[0090] The outputs of the delay elements 2a to 2d are supplied to multipliers 2e to 2h and assigned weights 2, 3, -2 and -1, respectively.

[0091] The outputs of the multipliers 2e to 2h are supplied to an adder 2i. The detection signal (2) is also supplied to the adder 2i.

[0092] The output of the adder 2i is then supplied to a 1/6 processor 2j and reduced by 1/6. The 1/6-reduced output (a correction signal) is supplied as the signal (3) to the adder 40 (FIG. 7).

[0093] The input video signal (1) is delayed by the delay unit 30 by a period that corresponds to two pixels and supplied to the adder 40 that outputs the signal (5).

[0094] The function of the block noise signal reduction apparatus shown in FIG. 7 is further explained with reference to FIGS. 10A to 10E.

[0095] The input video signal (1) having a gradation difference (noise) on the boundary between pixel blocks as shown in FIG. 10A is differentiated by the solitary differentiated point detector 10. The detector 10 outputs the detection signal (2) as shown in FIG. 10B that indicates the solitary differentiated point (c) of FIG. 8.

[0096] The detection signal (2) of FIG. 10B is filtered by the filter 20 as explained with reference to FIG. 9, to be the correction signal as shown in FIG. 10C, which is then supplied to the adder 40.

[0097] The input video signal (FIG. 10A) is delayed by the delay unit 30 by the period that corresponds to two pixels (2T) as shown in FIG. 10D and supplied to the adder 40.

[0098] The delayed video signal and the correction signal are added by the adder 40 which then outputs a corrected video signal as shown in FIG. 10E.

[0099] As described above, the noise reduction apparatus shown in FIG. 7 generates the correction signal (FIG. 10C) for canceling the gradation difference on the block boundary (FIG. 10A) for obtaining a smooth video signal with no abrupt step on the boundary as shown in FIG. 10E.

[0100] Another preferred embodiment of a block noise reduction apparatus according to the present invention is described with respect to FIG. 11.

[0101] Elements in the embodiment shown in FIG. 11 that are the same as or analogous to elements in the embodiment of FIG. 7 are referenced by the same reference numerals and will not be explained in detail.

[0102] The block noise reduction apparatus (FIG. 11) is provided with a block noise detection unit 50 and a switch 60 between the solitary differentiated point detector 10 and the filter 20.

[0103] Block noise reduction processing is made

on/off by the switch 60 according to the result of detection by the block noise detection unit 50.

[0104] As for the block noise detection unit 50, the integrator circuit 3 shown in FIG. 4, and the frame detector shown in FIG. 6 are employed in this embodiment.

[0105] When a block noise is generated on a video frame, the comparator 4b of the frame detector outputs the value "1" as explained with reference to FIG. 6. The value "1" is supplied to the switch 60 (FIG. 11) that allows the detection signal output by the solitary differentiated point detector 10 to pass therethrough and be supplied to the filter 20 for noise reduction.

[0106] On the other hand, when almost no block noise is generated, the comparator 4b outputs the value "0" which is then supplied to the switch 60. The switch 60 in this case outputs a zero-level signal for cutting off the noise reduction processing.

[0107] As explained with reference to FIG. 6, the median circuit 4e offers protection of reproduced images from chattering which would occur when the output of the comparator 4b changes frequently between "1" and "-1". This will be the cause of chattering of the switch 60 (FIG. 11).

[0108] Such frequent change in level occurs, for example, when block noises are generated on B frames but not on an I frame of a group of sequential B, B, I, B, B frames of a video signal according to the MPEG standard.

[0109] For such an MPEG video signal, the frame delay conducted by the delay circuits 4c and 4d (FIG. 6) applies the hysteresis characteristics to the output of the counter 4a and its middle value is output by the median circuit 4e. This avoids chattering of the switch 60 (FIG. 11) for reproducing images with less noises.

[0110] The present invention has been described in detail with reference to various hardware devices, however, it will be appreciated by those skilled in the art that the present invention can also be implemented in software which will be stored on a CD-ROM type storage medium or downloaded via net work, for example, to cause a computer to detect and/or reduce block noises generated on video signals.

[0111] As disclosed above, according to the present invention, block noises are detected by differentiating input video signals for obtaining solitary differentiated points and integrating the points.

[0112] The present invention thus achieves precise block noise detection even though boundaries between pixel blocks are unknown.

[0113] The precise block noise detection is further achieved by integration processing in both the horizontal and the vertical directions for generating impulses that have correlation with block noise in both directions.

[0114] Furthermore, as disclosed above, according to the present invention, block noises are reduced by differentiating input video signals to obtain solitary differentiated points for generating correction signals for canceling differences in signal levels on pixel block boundaries.

[0115] The present invention thus achieves block noise reduction with relatively small circuitry.

[0116] Moreover, the block noise reduction processing according to the present invention is applied only to video frames on which many block noises are generated to avoid chartering.

[0117] The present invention thus achieves block noise reduction with the least deterioration of images.

Claims

1. An apparatus for detecting a block noise generated on an input video signal that has been code and decoded per pixel block, the apparatus comprising:

   a differentiator to differentiate the input video signal per pixel block to obtain a differentiated signal;
   a detector to detect impulses of the differentiated signal to obtain a detection signal carrying the impulses;
   an integrator to integrate the detection signal; and
   a determinator to compare the integrated detection signal and a reference signal to determine whether the block noise is generated on the input video signal.

2. The apparatus according to claim 1 wherein each pixel block has a predetermined number of pixels in both the horizontal and the vertical directions of the pixel block, the integrator integrating the detection signal in the horizontal and the vertical directions for a period corresponding to the pixel block.

3. The apparatus according to claim 2 wherein the determinator includes:

   a counter to count the number of integrated impulses of the integrated detection signal per predetermined unit of image carried by the input video signal;
   a plurality of delay sections each delaying the counted number by a period decided based on the predetermined unit of image, thus outputting count signals for succeeding images in the predetermined unit of image; and
   a median section to select a middle count signal among the count signals, which is the middle in level, the middle count signal being compared with the reference signal.

4. An apparatus for reducing a block noise generated on an input video signal that has been code and decoded per pixel block, the apparatus comprising:

a differentiator to differentiate the input video signal per pixel block to obtain a differentiated signal and detect impulses of the differentiated signal, thus outputting a detection signal carrying the impulses;
a filter to filter the detection signal to obtain a correction signal;;
a delay section to delay the input video signal by a predetermined period; and
an adder to add the correction signal to the delayed video signal to cancel a difference in signal level on the boundary between a first pixel block on which a block noise is generated and a second pixel block adjacent to the first pixel block of the input video signal.

5. The apparatus according to claim 4 further comprising:

a detector to detect the block noise per predetermined unit of image carried by the input video signal; and
a switch to pass the detection signal carrying the impulses to the filter when the block noise is detected.

6. The apparatus according to claim 5 wherein each pixel block has a predetermined number of pixels in both the horizontal and the vertical directions of the pixel block, the detector including:

an integrator to integrate the detection signal in the horizontal and the vertical directions for a period corresponding to the pixel block; and
a determinator to compare the integrated detection signal and a reference signal to determinate whether the block noise is generated.

7. The apparatus according to claim 6 wherein the determinator includes:

a counter to count the number of integrated impulses of the integrated detection signal per predetermined unit of image carried by the video signal;
a plurality of delay sections each delaying the counted number by a period decided based on the predetermined unit of image, thus outputting count signals for succeeding images in the predetermined unit of image; and
a median section to select a middle count signal among the count signals, which is the middle in level, the middle count signal being compared with the reference signal.

8. A method of detecting a block noise generated on an input video signal that has been code and decoded per pixel block, comprising the steps of:

differentiating the input video signal per pixel block to obtain a differentiated signal;
detecting impulses of the differentiated signal to obtain a detection signal carrying the impulses;
integrating the detection signal; and
comparing the integrated detection signal and a reference signal to determine whether the block noise is generated on the input video signal.

9. The method according to claim 8 wherein each pixel block has a predetermined number of pixels in both the horizontal and the vertical directions of the pixel block, the integrating step including the step of integrating the detection signal in the horizontal and the vertical directions for a period corresponding to the pixel block.

10. The method according to claim 9 wherein the comparing step includes the steps of:

counting the number of integrated impulses of the integrated detection signal per predetermined unit of image carried by the input video signal;
delaying the counted number by a period decided based on the predetermined unit of image, thus outputting count signals in the predetermined unit of image; and
selecting a middle count signal among the count signals, which is the middle in level, the middle count signal being compared with the reference signal.

11. A method of reducing a block noise generated on an input video signal that has been code and decoded per pixel block, comprising the steps of:

differentiating the input video signal per pixel block to obtain a differentiated signal and detect impulses of the differentiated signal, thus outputting a detection signal carrying the impulses;
filtering the detection signal to obtain a correction signal;
delaying the input video signal by a predetermined period; and
adding the correction signal to the delayed video signal to cancel a difference in signal level on the boundary between a first pixel block on which a block noise is generated and a second pixel block adjacent to the first pixel block of the input video signal.

12. The method according to claim 11 further compris-

ing the steps of:

detecting the block noise per predetermined unit of image carried by the input video signal; and

passing the detection signal carrying the impulses to the filter when the block noise is detected.

13. A computer-implemented method of detecting a block noise generated on an input video signal that has been code and decoded per pixel block, comprising the steps of:

differentiating the input video signal per pixel block to obtain a differentiated signal;

detecting impulses of the differentiated signal to obtain a detection signal carrying the impulses;

integrating the detection signal; and

comparing the integrated detection signal and a reference signal to determine whether the block noise is generated on the input video signal.

14. A computer-implemented method of reducing a block noise generated on an input video signal that has been code and decoded per pixel block, comprising the steps of:

differentiating the input video signal per pixel block to obtain a differentiated signal and detect impulses of the differentiated signal, thus outputting a detection signal carrying the impulses;

filtering the detection signal to obtain a correction signal;

delaying the input video signal by a predetermined period; and

adding the correction signal to the delayed video signal to cancel a difference in signal level on the boundary between a first pixel block on which a block noise is generated and a second pixel block adjacent to the first pixel block of the input video signal.

15. A processor readable medium storing program code for causing a computer to detect a block noise generated on an input video signal that has been code and decoded per pixel block, comprising:

first program code means for differentiating the input video signal per pixel block to obtain a differentiated signal;

second program code means for detecting impulses of the differentiated signal to obtain a detection signal carrying the impulses;

third program code means for integrating the detection signal; and

fourth program code means for comparing the integrated detection signal and a reference signal to determine whether the block noise is generated on the input video signal.

16. A processor readable medium storing program code for causing a computer to reduce a block noise generated on an input video signal that has been code and decoded per pixel block, comprising:

first program code means for differentiating the input video signal per pixel block to obtain a differentiated signal and detect impulses of the differentiated signal, thus outputting a detection signal carrying the impulses;

second program code means for filtering the detection signal to obtain a correction signal;

third program code means for delaying the input video signal by a predetermined period; and

fourth program code means for adding the correction signal to the delayed video signal to cancel a difference in signal level on the boundary between a first pixel block on which a block noise is generated and a second pixel block adjacent to the first pixel block of the input video signal.

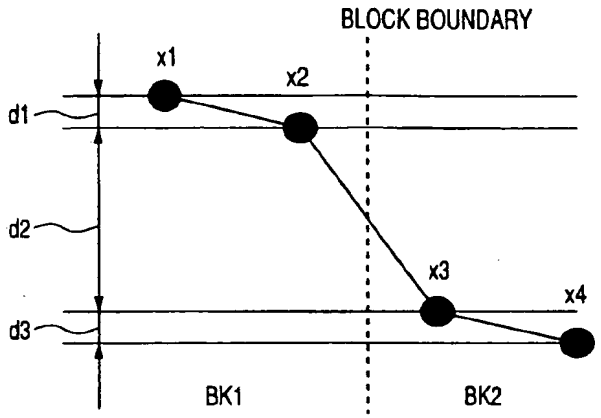


FIG.1 RELATED ART

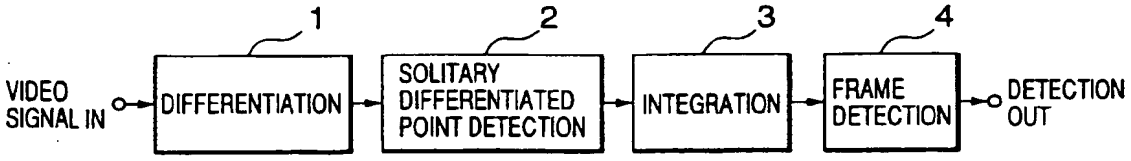
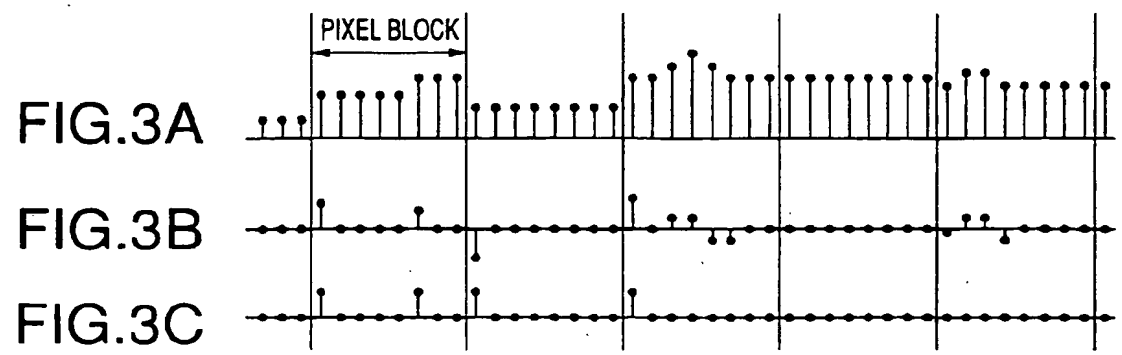


FIG.2

FIG.3A

FIG.3B

FIG.3C



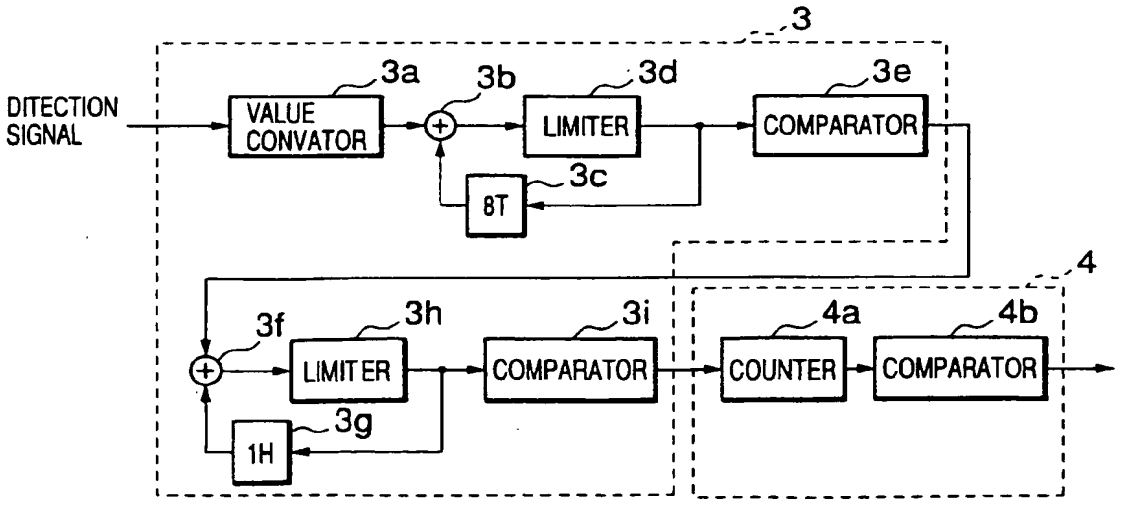


FIG.4

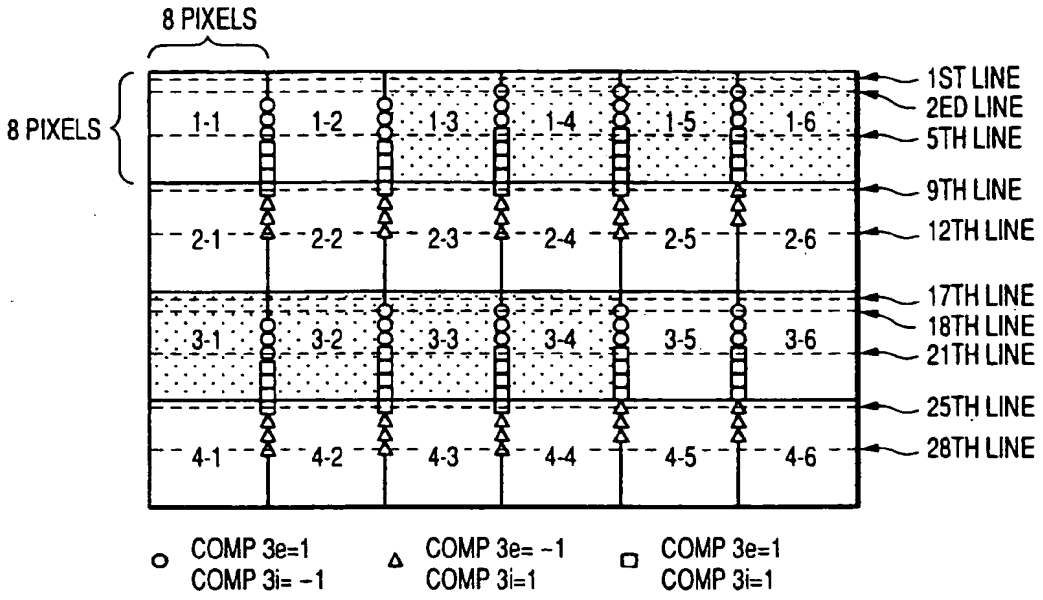

8 PIXELS
8 PIXELS
1-1
1-2
1-3
1-4
1-5
1-6
2-1
2-2
2-3
2-4
2-5
2-6
3-1
3-2
3-3
3-4
3-5
3-6
4-1
4-2
4-3
4-4
4-5
4-6
1ST LINE
2ED LINE
5TH LINE
9TH LINE
12TH LINE
17TH LINE
18TH LINE
21TH LINE
25TH LINE
28TH LINE
COMP 3e=1
COMP 3i= -1
COMP 3e= -1
COMP 3i=1
COMP 3e=1
COMP 3i=1

FIG.5

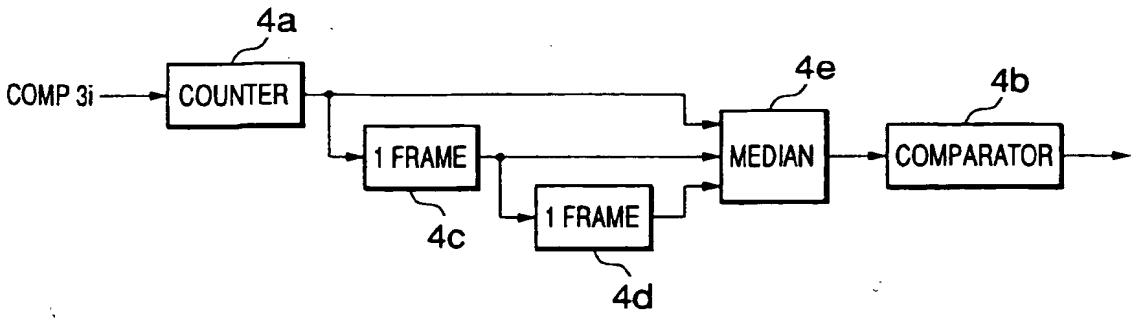

4a
COMP 3i
COUNTER
1 FRAME
4c
1 FRAME
4d
4e
MEDIAN
4b
COMPARATOR

FIG.6

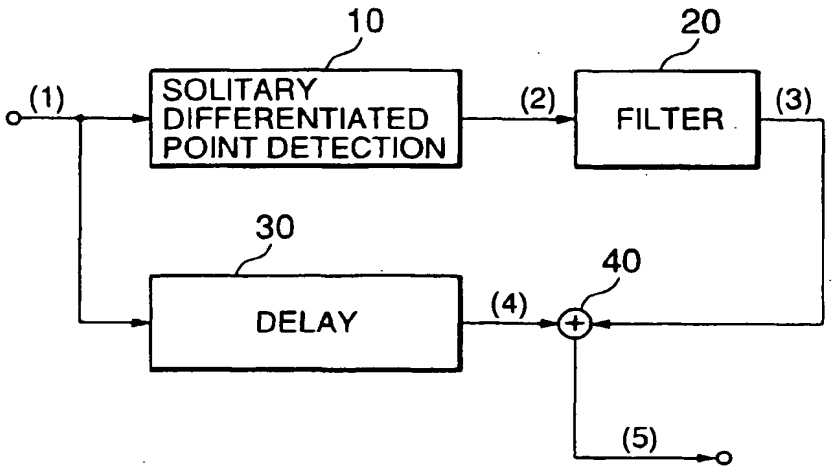
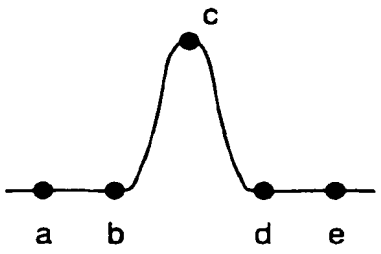


FIG.7



$|c-d| > |d-e|$ AND $|b-c| > |a-b|$ BUT NOT
$b \leqq c \leqq d$ AND $b \geqq c \geqq d$

FIG.8

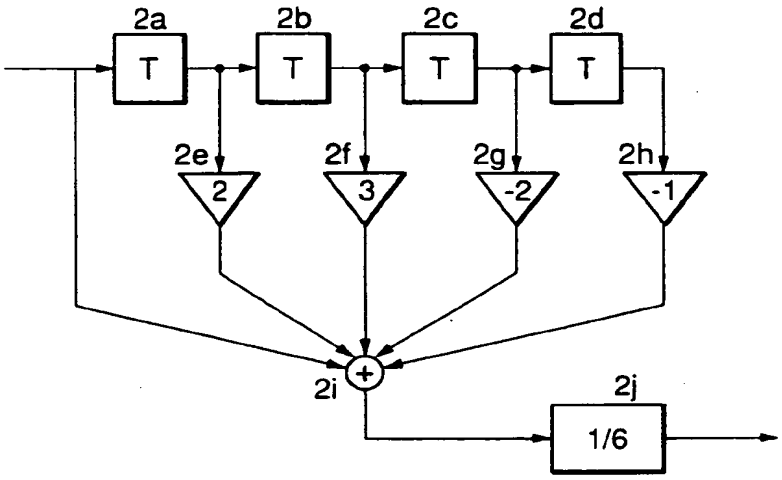


FIG.9

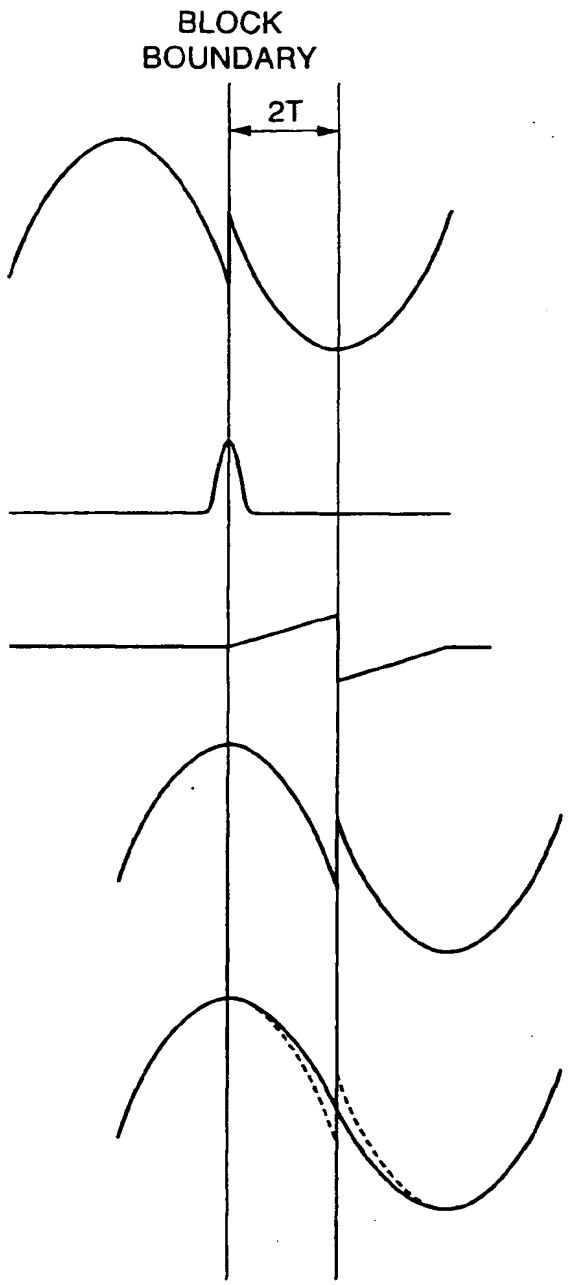
FIG. 10A

FIG. 10B

FIG. 10C

FIG. 10D

FIG. 10E



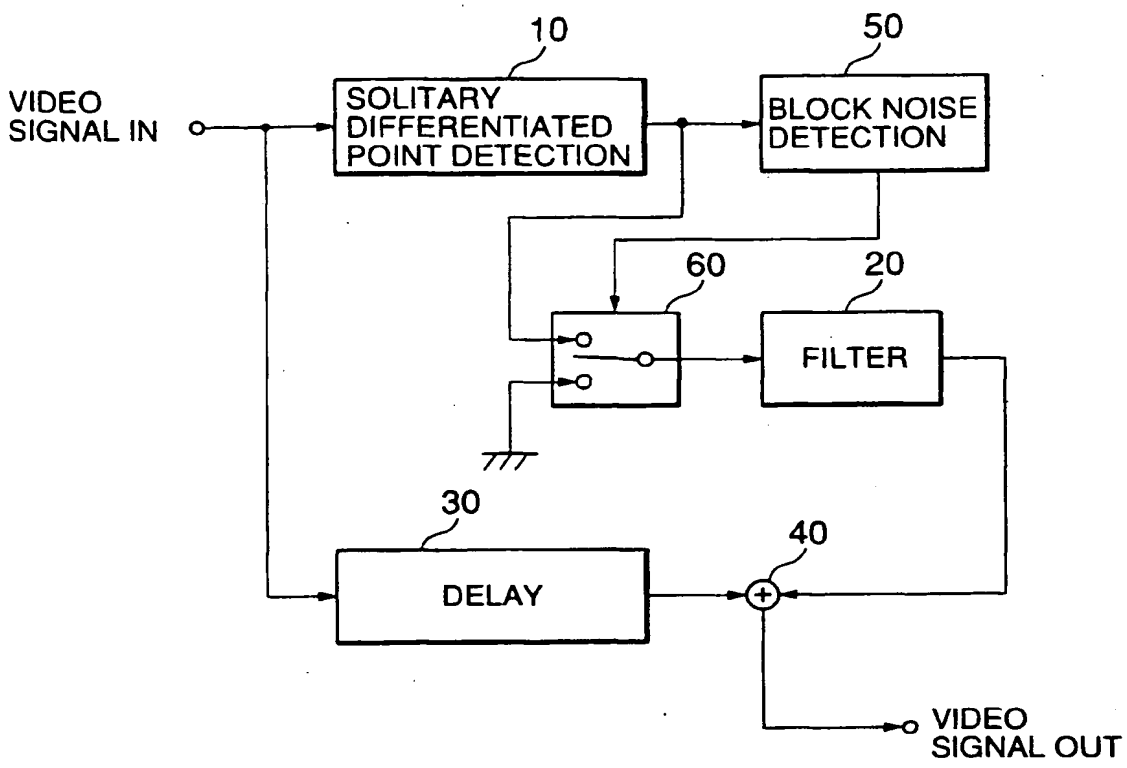

10
50
VIDEO
SIGNAL IN
SOLITARY
DIFFERENTIATED
POINT DETECTION
BLOCK NOISE
DETECTION
60
20
FILTER
30
40
DELAY
VIDEO
SIGNAL OUT

FIG. 11